REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow. Claims 1-4, 7-9, and 17 have been amended. No new matter has been added. Accordingly, Claims 1-20 remain pending in the application.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

Claim Rejections – 35 U.S.C. § 102(b)

On page 6 of the Office Action, Claims 7 and 12-16 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,187,682 to Denning et al. On page 9 of the Office Action, Claim 17 was rejected under 35 U.S.C. § 102(b) as being anticipated by Denning et al. The Applicants respectfully traverse these rejections.

Independent Claim 7 (as amended) recites a "method of pre-cleaning a top surface of an IC substrate" that includes "exposing the IC substrate to hydrofluoric acid to remove native oxide from the IC substrate; and providing a plasma including hydrogen in the chamber to remove native oxide from the IC substrate remaining after the exposure of the IC substrate to hydrofluoric acid."

Independent Claim 17 (as amended) recites a "method of manufacturing a transistor on an integrated circuit" that includes, among other limitations, "providing a gate structure on a top surface of a strained silicon layer or a silicon germanium layer; removing a native oxide material from the strained silicon layer or silicon germanium layer using a hydrofluoric acid wet bath" and "providing a plasma including hydrogen and argon to remove the native oxide material."

Denning et al. does not identically disclose the methods recited in independent Claims 7 and 17, as amended herein. In contrast, Denning et al. relates to an "inert plasma gas

surface cleaning process" and discloses that an "inert gas, noble gas, or a reducing gas is introduced into the semiconductor processing chamber" (column 3, lines 3-5). "A coil internal to the chamber is radio frequency (RF) powered to create a plasma from the gas whereby charged ions from the input inert, noble or reducing gas are generated" (column 3, lines 5-8).

As acknowledged by the Examiner on page 5 of the Office Action, Denning et al. does not disclose "utilizing an HF dip." Accordingly, Denning et al. does not disclose "exposing the IC substrate to hydrofluoric acid to remove native oxide from the IC substrate" as recited in independent Claim 7 (as amended) or "removing a native oxide material from the strained silicon layer or silicon germanium layer using a hydrofluoric acid wet bath" as recited in independent Claim 17 (as amended).

The rejection of Claims 7 and 12-17 should be withdrawn, because at least one limitation of independent Claim 7 and Claim 17 (as amended) is not identically disclosed by Denning et al. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 7 and 12-17 under 35 U.S.C. § 102(b).

Claim Rejections – 35 U.S.C. § 103(a)

1. Claims 1-2 and 5-6

On page 2 of the Office Action, Claims 1-2 and 5-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Denning et al. in view of U.S. Patent No. 6,486,520 to Okuno et al. Applicants respectfully traverse these rejections.

Independent Claim 1 (as amended) recites a "method of manufacturing an integrated circuit" that includes, among other limitations, "providing a substrate, the substrate including a layer including germanium; providing a gate structure above the substrate; pre-cleaning the substrate using hydrofluoric acid after the step of providing a gate structure; and pre-cleaning the substrate with an argon and hydrogen plasma after the step of pre-cleaning the substrate using hydrofluoric acid."

As described above, Denning et al. relates to an "inert plasma gas surface cleaning process" and discloses that an "inert gas, noble gas, or a reducing gas is introduced into the semiconductor processing chamber" (column 3, lines 3-5). "A coil internal to the chamber is radio frequency (RF) powered to create a plasma from the gas whereby charged ions from the input inert, noble or reducing gas are generated" (column 3, lines 5-8). Okuno et al. relates to a "structure and method for a large-permittivity gate using a germanium layer."

Neither Denning et al. nor Okuno et al., alone or in any proper combination, teach or suggest all elements of independent Claim 1 (as amended). For example, as acknowledged by the Examiner, Denning et al. does not disclose "utilizing an HF dip." Accordingly, Denning et al. does not teach or suggest "pre-cleaning the substrate using hydrofluoric acid after the step of providing a gate structure," as recited in Claim 1. Nor does the combination of Denning et al. with Okuno et al. provide the necessary teaching or suggestion to provide the step of "pre-cleaning the substrate using hydrofluoric acid after the step of providing a gate structure," as recited in Claim 1. Accordingly, the combination of Denning et al. and Okuno et al. fail to teach or suggest at least one element recited in Claim 1.

The rejection of Claims 1-2 and 5-6 should be withdrawn, because at least one limitation of independent Claim 1 is not taught or suggested by the combination of Denning et al. and Okuno et al. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 1-2 and 5-6 under 35 U.S.C. § 103(a).

2. Claims 8-11 and 18-20

On page 7 of the Office Action, Claims 8-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Denning et al. in view of U.S. Patent No. 5,403,434 to Moslehi. On page 10, Claims 18-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Denning et al. in view of Moslehi. Applicants respectfully traverse these rejections.

Independent Claim 7 (as amended) recites a "method of pre-cleaning a top surface of an IC substrate" that includes "exposing the IC substrate to hydrofluoric acid to remove native oxide from the IC substrate; and providing a plasma including hydrogen in the

chamber to remove native oxide from the IC substrate remaining after the exposure of the IC substrate to hydrofluoric acid."

Independent Claim 17 (as amended) recites a "method of manufacturing a transistor on an integrated circuit" that includes, among other limitations, "providing a gate structure on a top surface of a strained silicon layer or a silicon germanium layer; removing a native oxide material from the strained silicon layer or silicon germanium layer using a hydrofluoric acid wet bath" and "providing a plasma including hydrogen and argon to remove the native oxide material."

Neither Denning et al. nor Moslehi, alone or in any proper combination, teach or suggest using both hydrofluoric acid and a plasma including hydrogen (Claim 7) or a plasma including hydrogen and argon (Claim 17) to clean a substrate. In contrast, Denning et al. discloses that an "inert gas, noble gas, or a reducing gas is introduced into the semiconductor processing chamber" (column 3, lines 3-5) and that "A coil internal to the chamber is radio frequency (RF) powered to create a plasma from the gas whereby charged ions from the input inert, noble or reducing gas are generated" (column 3, lines 5-8). Denning et al. does not teach or suggest the use of hydrofluoric acid.

Moslehi relates to a "low-temperature dry cleaning process for semiconductor wafer" and states the following at column 1, lines 51-62:

> A conventional procedure for removing surface contaminants and native oxides prior to epitaxial silicon growth processes and some gate dielectric formation processes involves an ex-situ aqueous cleaning (such as the so-called RCA cleaning followed by a final HF dip), followed by an in-situ high-temperature (around 1000°C to 1200°C) H_2 bake. The wet clean step is expected to remove most of the native oxide and other trace contaminants, while the high-temperature H_2 prebake removes the residual native oxide layer left on the semiconductor surface due to ambient exposure during wafer transport to the fabrication equipment.

There is no teaching or suggestion in either Denning et al. or Moslehi to utilize both the plasma process disclosed in Denning et al. with the HF dip process disclosed in Moslehi to process the same substrates. Nevertheless, the Examiner concluded (emphasis in original):

> It would have been obvious to one having ordinary skill in the art to use wet clean as cited in Moslehi in addition of plasma clean as disclosed in Denning in pre-cleaning process to remove native oxides **because** the wet clean follow by plasma clean before depositing films on the substrate would reduce contact resistance, improve uniformity and conductivity, and reduce the manufacturing cost. The wet clean removes contaminants and most of native oxides at a lower cost and faster process but doesn't remove the native oxides that grow when the substrate is exposed to the air due to ambient exposure during wafer transport from the wet clean bath to the fabrication equipment (Moslehi, lines 50-60, Col. 1; lines 10-14, Col. 2), meanwhile, plasma clean (higher cost and slower process) disclosed in Denning et al. using the same chamber for both plasma cleaning and depositing film removes all native oxides that grow when the substrate is exposed to the air to avoid adversely effect subsequent processing steps, for example, causing high contact resistance or impeding interfacial reactions of films deposited on the substrate materials.

It is unclear to the Applicants where the Examiner has found this asserted motivation to combine the teachings of Denning et al. with those of Moslehi, as such motivation is not stated in either Denning et al. or Moslehi. In fact, Moslehi teaches away from such a result when it states, as indicated above, that the "wet clean step is expected to remove most of the native oxide and other trace contaminants, while the high-temperature H_2 prebake removes the residual native oxide layer left on the semiconductor surface due to ambient exposure during wafer transport to the fabrication equipment." Thus, rather that teaching the use of a subsequent hydrogen or hydrogen/plasma cleaning step, Moslehi teaches an entirely different step with no reference to hydrogen or hydrogen/plasma cleaning. Further, while Moslehi does describe an "alternative" process at column 3, lines 35-42 that uses a plasma, there is no teaching or suggestion that such alternative process could be used in conjunction with the "HF dip" described at column 1, lines 50-62.

Accordingly, the Applicants submit that the Examiner has not satisfied the burden of establishing some teaching or motivation to one of ordinary skill in the art to combine the teachings of the references in the manner suggested in the Office Action, and that the rejection of Claims 8-11 and 18-20 should be withdrawn. The only teaching or suggestion to utilize both hydrofluoric acid and a plasma including hydrogen (Claim 7) or a plasma including hydrogen and argon (Claim 17) to clean a substrate comes from the Applicants' own disclosure. As noted in M.P.E.P. § 2143.01, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

The rejection of Claims 8-11 and 18-20 should be withdrawn, because the Examiner has not established that one of ordinary skill in the art would have been motivated to combine the teachings of Denning et al. with those of Moslehi. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 8-11 and 18-20 under 35 U.S.C. § 103(a).

3. Claims 3-4

On page 4, Claims 3-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Denning et al. in view of Okuno et al. and Moslehi et al. Applicants respectfully traverse these rejections.

Independent Claim 1 (as amended) recites a "method of manufacturing an integrated circuit" that includes, among other limitations, "providing a substrate, the substrate including a layer including germanium; providing a gate structure above the substrate; pre-cleaning the substrate using hydrofluoric acid after the step of providing a gate structure; and pre-cleaning the substrate with an argon and hydrogen plasma after the step of pre-cleaning the substrate using hydrofluoric acid."

There is no teaching or suggestion in any of the cited references to combine the teachings of Moslehi with those of Denning et al. or Okuno et al. The Office Action includes the same reasoning for making such a combination as described in the preceding section of this Reply. As described above, it appears that the Examiner has not satisfied the burden of

establishing that there is some teaching or motivation to one of ordinary skill in the art to combine the teachings of the references in the manner suggested in the Office Action.

The only teaching or suggestion to utilize both hydrofluoric acid and a plasma including hydrogen (Claim 7) or a plasma including hydrogen and argon (Claim 17) to clean a substrate comes from the Applicants' own disclosure.

The rejection of Claims 3-4 should be withdrawn, because the Examiner has not established that one of ordinary skill in the art would have been motivated to combine the teachings of Moslehi with those of the other cited references. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claims 3-4 under 35 U.S.C. § 103(a).

* * *

It is submitted that each outstanding objection and rejection to the Application has been overcome, and that the Application is in a condition for allowance. Claims 1-20 will be pending in this Application. The Applicants request consideration and allowance of all pending Claims 1-20.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

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